THE INVENTION CLAIMED IS:

1. A method for writing a least recently used (LRU) indicator comprising:

activating one of a first word line that corresponds to a first memory array and a second word line which corresponds to a second memory array;

employing the first word line, when activated, for writing to the first memory array and for writing the LRU indicator; and

employing the second word line, when activated, for writing to the second memory array and for writing the LRU indicator.

2. The method of claim 1 further comprising setting a signal on a first and second bit line to a first logic state.

3. The method of claim 2 wherein setting a signal on the first and second bit line to a first logic state includes setting a signal on the first and second bit line to a low logic state.

4. The method of claim 1 wherein activating one of the first word line that corresponds to the first memory array and the second word line which corresponds to the second memory array includes setting a signal on one of the first word line and the second word line to a second logic state.

5. The method of claim 4 wherein setting a signal on one of the first word line and the second word line to a second logic state includes setting a signal on one of the first word line and the second word line to a high logic state.

6. The method of claim 1 wherein employing the first word line, when activated, for writing to the first memory array and for writing the LRU indicator includes employing the first word line, when activated, for writing to the first memory array and for activating a first port of a cell that stores the LRU indicator; and

wherein employing the second word line, when activated, for writing to the second memory array and for writing the LRU indicator includes employing the second word line, when activated, for writing to the second memory array and for activating a second port of the cell that stores the LRU indicator.

7. The method of claim 1 wherein employing the first word line, when activated, for writing to the first memory array and for writing the LRU indicator includes employing the first word line, when activated, for writing to the first memory array and for storing a bit of a first logic state in a cell that stores the LRU indicator; and

wherein employing the second word line, when activated, for writing to the second memory array and for writing the LRU indicator includes employing the second word line, when activated, for writing to the second memory array and for storing a bit of a second logic state in the cell that stores the LRU indicator.

8. An apparatus for writing an LRU indicator comprising:

a first memory array coupled to a first word line and a first bit line;

a second memory array coupled to a second word line and a second bit line;

a cell for storing the LRU indicator coupled to the first and second memory arrays;

an integrated circuit (IC) coupled to the first and second memory arrays, and adapted to:

activate one of the first word line and the second word line;

employ the first word line, when activated, for writing to the first memory array and for writing the LRU indicator; and

employ the second word line, when activated, for writing to the second memory array and for writing the LRU indicator.

9. The apparatus of claim 8 wherein the IC is further adapted to set a signal on the first and second bit lines to a first logic state.

10. The apparatus of claim 9 wherein the IC is further adapted to set a signal on the first and second bit line to a low logic state.

11. The apparatus of claim 8 wherein the IC is further adapted to set a signal on one of the first word line and the second word line to a second logic state.

12. The apparatus of claim 11 wherein the IC is further adapted to set a signal on one of the first word line and the second word line to a high logic state.

13. The apparatus of claim 8 wherein the IC is further adapted to:

employ the first word line, when activated, for writing to the first memory array and for activating a first port of the cell that stores the LRU indicator; and

employ the second word line, when activated, for writing to the second memory array and for activating a second port of the cell that stores the LRU indicator.

14. The apparatus of claim 8 wherein the IC is further adapted to:

employ the first word line, when activated, for writing to the first memory array and for storing a bit of a first logic state in the cell that stores the LRU indicator; and

employ the second word line, when activated, for writing to the second memory array and for storing a bit of a second logic state in the cell that stores the LRU indicator.

15. The apparatus of claim 8 wherein the cell is included in a pass-gate circuit.

16. The apparatus of claim 15 wherein the cell is a node at an input of a first logic device and an output of a second logic device of the pass-gate circuit.

17. The apparatus of claim 15 wherein the cell is a node at an output of a first logic device and an input of a second logic device of the pass-gate circuit.